

# Refine Search

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| <u>L1</u>                                    | (bus near5 arbit\$6) and (grant\$3 same (concurrent\$2 or simultaneous\$2) same latenc\$3) | 14                         | <u>L1</u>                               |

END OF SEARCH HISTORY

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Search Results -

| Terms  | Documents |
|--|-----------|
| (bus near5 arbit\$6) and (grant\$3 same (concurrent\$2 or simultaneous\$2) same latenc\$3) | 59        |

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|  | DB=PGPB,USPT,USOC; PLUR=YES; OP=OR   |                            |   |
| <u>L1</u>                                    | (bus near5 arbit\$6) and (grant\$3 same (concurrent\$2 or simultaneous\$2) same latenc\$3) | 59                         | <u>L1</u>                               |

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Search Results -

| Terms  | Documents |
|--|-----------|
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Search:

L2

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|--|--|----------------------------|---|
| <i>DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i> |  |                            |   |
| <u>L2</u>                                      | (bus near5 arbit\$6) and (grant\$3 same (concurrent\$2 or simultaneous\$2) same latenc\$3) | 11                         | <u>L2</u>                               |
| <i>DB=PGPB,USPT,USOC; PLUR=YES; OP=OR</i>      |  |                            |   |
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| Terms   | Documents |
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Search:

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DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L3    710/110,113,40,107,305,244,36,40,58,112,48;370/461,462;340/825.5,825.51;711/147,100.ccls.    9646    L3

DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L2    (bus near5 arbit\$6) and (grant\$3 same (concurrent\$2 or simultaneous\$2) same latenc\$3)    11    L2

DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L1    (bus near5 arbit\$6) and (grant\$3 same (concurrent\$2 or simultaneous\$2) same latenc\$3)    59    L1

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### Search Results -

| Terms     | Documents |
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|---|----------------------------|--|
| <i>DB=PGPB,USPT,USOC; PLUR=YES; OP=OR</i>   |                            |  |
| <u>L4</u> 11 and L3   | 37                         | <u>L4</u>                                  |
| <u>L3</u> 710/110,113,40,107,305,244,36,40,58,112,48;370/461,462;340/825.5,825.51;711/147,100.ccls.<br><i>DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i> | 9646                       | <u>L3</u>                                  |
| <u>L2</u> (bus near5 arbit\$6) and (grant\$3 same (concurrent\$2 or simultaneous\$2) same latenc\$3)<br><i>DB=PGPB,USPT,USOC; PLUR=YES; OP=OR</i>     | 11                         | <u>L2</u>                                  |
| <u>L1</u> (bus near5 arbit\$6) and (grant\$3 same (concurrent\$2 or simultaneous\$2) same latenc\$3)  | 59                         | <u>L1</u>                                  |

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### Search Results -

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| L1 and L2 | 1         |

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L3





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|--|--|----------------------------|---|
|  | <i>DB=PGPB,USPT,USOC; PLUR=YES; OP=OR</i>  |                            |   |
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| <u>L2</u>                                    | (bus near5 arbit\$6) and (grant\$3 same (concurrent\$2 or simultaneous\$2) same latenc\$3) | 59                         | <u>L2</u>                               |
| <u>L1</u>                                    | 710/111.ccls.  | 112                        | <u>L1</u>                               |

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Highlight all hit terms initially

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IS&R form

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|---|--------------------------|--------------------------|---------------|-----------|-------|--|------------|----------------------|
| 1 | <input type="checkbox"/> | <input type="checkbox"/> | US 6173349 B1 | 20010109  | 15    | Shared bus system with transaction and destina | 710/110    | 710/107;<br>710/113; |





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Citation



Citation &amp; Abstract

IEEE JNL IEEE Journal or Magazine

IEEE JNL IEEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEEE Conference Proceeding

IEEE STD IEEE Standard

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## » Key

|          |                            |
|----------|----------------------------|
| IEEE JNL | IEEE Journal or Magazine   |
| IEE JNL  | IEE Journal or Magazine    |
| IEEE CNF | IEEE Conference Proceeding |
| IEE CNF  | IEE Conference Proceeding  |
| IEEE STD | IEEE Standard              |

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Ruibing Lu; Cheng-Koh Koh;  
[Computer Aided Design, 2003, ICCAD-2003, International Conference on](#)  
9-13 Nov. 2003 Page(s):8 - 12  
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- ☐ 2. **Performance model for a prioritized multiple-bus multiprocessor system**  
John, L.K.; Yu-Cheng Liu;  
[Computers, IEEE Transactions on](#)  
Volume 45, Issue 5, May 1996 Page(s):580 - 588  
Digital Object Identifier 10.1109/12.509909  
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- ☐ 3. **Resolving the Fairness Issues in Bus-Based Optical Access Networks**  
Bouabdallah, N.; Beylot, A.-L.; Dotaro, E.; Pujolle, G.;  
[Selected Areas in Communications, IEEE Journal on](#)  
Volume 23, Issue 8, Aug. 2005 Page(s):1444 - 1457  
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- ☐ 4. **Design of a CMOS buffered switch for a Gigabit ATM switching network**  
Mirfakhraei, N.;  
[Solid-State Circuits, IEEE Journal of](#)  
Volume 30, Issue 1, Jan. 1995 Page(s):11 - 18  
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- ☐ 5. **Resolving the fairness issue in bus-based optical access networks**  
Bouabdallah, N.; Dotaro, E.; Ciavaglia, L.; Le Sauze, N.; Pujolle, G.;  
[Communications Magazine, IEEE](#)  
Volume 42, Issue 11, Nov. 2004 Page(s):S12 - S18  
Digital Object Identifier 10.1109/MCOM.2004.1362545  
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(289 KB) [IEEE JNL](#)  
[Rights and Permissions](#)
- ☐ 6. **Performance model for a prioritized multiple-bus multiprocessor system**

Kurian, L.; Yu-Cheng Liu;  
Parallel and Distributed Processing, 1994. Proceedings. Sixth IEEE Symposium on  
 26-29 Oct. 1994 Page(s):577 - 584  
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☐ **7. A fluid flow tracking arbiter for input buffered ATM switch with heterogeneous port bandwidth**

Vishnu, M.;  
Global Telecommunications Conference, 2003. GLOBECOM '03. IEEE  
 Volume 6, 1-5 Dec. 2003 Page(s):3138 - 3143 vol.6  
 Digital Object Identifier 10.1109/GLOCOM.2003.1258814  
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☐ **8. The multiprocessor system with a fairly weighted global bus arbitration circuit**

Deshmukh, R.G.; Doi, S.;  
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 1-4 April 1990 Page(s):750 - 754 vol.2  
 Digital Object Identifier 10.1109/SECON.1990.117917  
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☐ **9. Point-to-point connectivity between neuromorphic chips using address events**

Boahen, K.A.;  
Circuits and Systems II: Analog and Digital Signal Processing. IEEE Transactions on [see also Circuits and Systems II: Express Briefs. IEEE Transactions on]  
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 Digital Object Identifier 10.1109/82.842110  
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☐ **10. Architecture and performance comparison of a statistic-based lottery arbiter for shared bus on chip**

Yan Zhang;  
Design Automation Conference, 2005. Proceedings of the ASP-DAC 2005. Asia and South Pacific  
 Volume 2, 18-21 Jan. 2005 Page(s):1313 - 1316 Vol. 2  
 Digital Object Identifier 10.1109/ASPDAC.2005.1466585  
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Petro, F.; Hommais, D.;  
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 Volume 5, 28-31 May 2000 Page(s):749 - 752 vol.5  
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☐ **12. Some solutions for FIP network interconnection**

Saba, G.; Mammeri, Z.; Thomesse, J.P.;  
Factory Communication Systems, 1995. WFCS '95. Proceedings. 1995 IEEE International Workshop on  
 4-6 Oct. 1995 Page(s):13 - 20  
 Digital Object Identifier 10.1109/WFCS.1995.482645  
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☐ **13. Ordered arbiters**

Bystrov, A.; Yakovlev, A.;  
Electronics Letters  
 Volume 35, Issue 11, 27 May 1999 Page(s):877 - 879  
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[Bystrov, A. Yakovlev, A.](#)

Dept. of Comput. Sci., Newcastle upon Tyne Univ., UK

This paper appears in: [Electronics Letters](#)

Publication Date: 27 May 1999

Volume: 35, Issue: 11

On page(s): 877 - 879

ISSN: 0013-5194

INSPEC Accession Number: 6278050

Posted online: 2003-07-09 09:39:02.0

## Abstract

The granting of requests in the order of their arrival is not satisfied in existing 1/n arbiters, such as token rings, tree arbiters and networks of two-way arbiters. The proposed solution stores pending grants in a FIFO, thus maximally preserving the request order, improves fairness and offers lower metastability rate.

## Index Terms

## Inspec

## Controlled Indexing

[network interfaces](#)

## Non-controlled Indexing

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